EUV Lithography for High-Volume Manufacturing

Progress and Challenges

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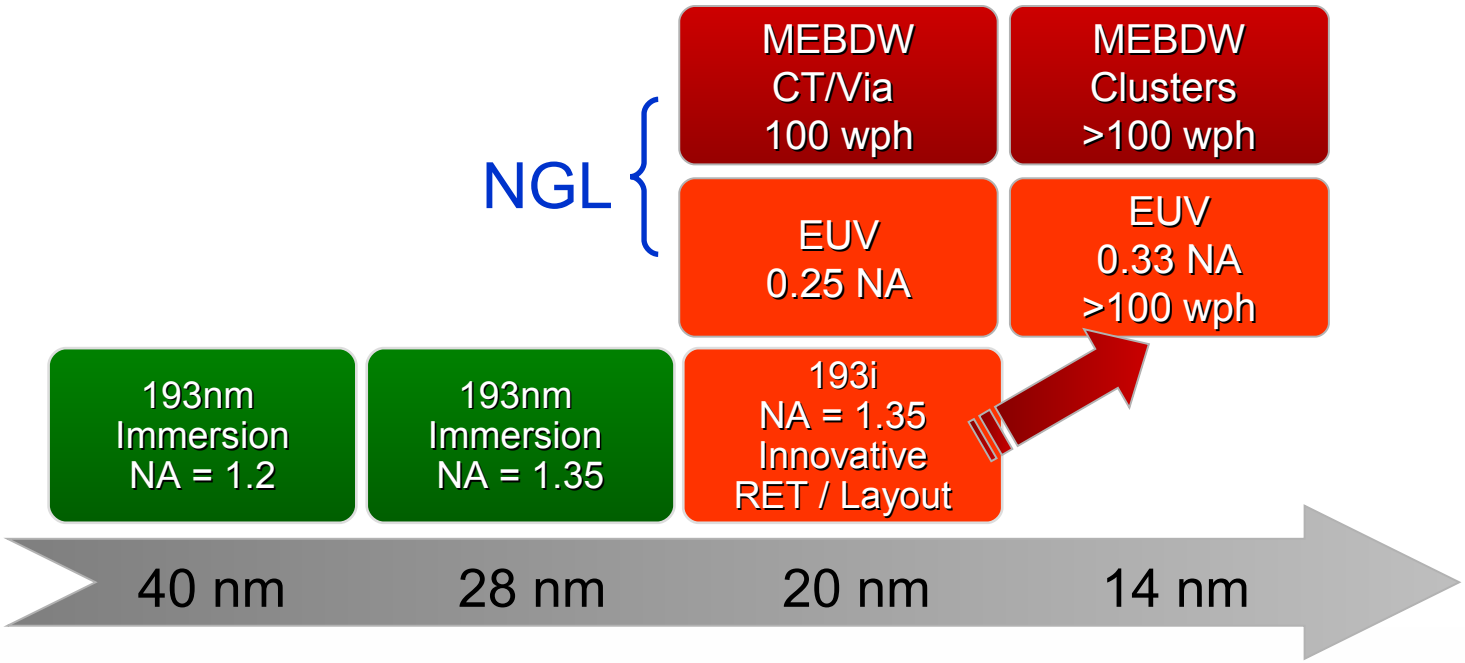
TSMC Lithography Roadmap

- 28 nm is the limit of conventional single-patterning lithography
- TSMC has innovations to extend immersion to 20 nm
- NGL technologies are preferred beyond 20 nm

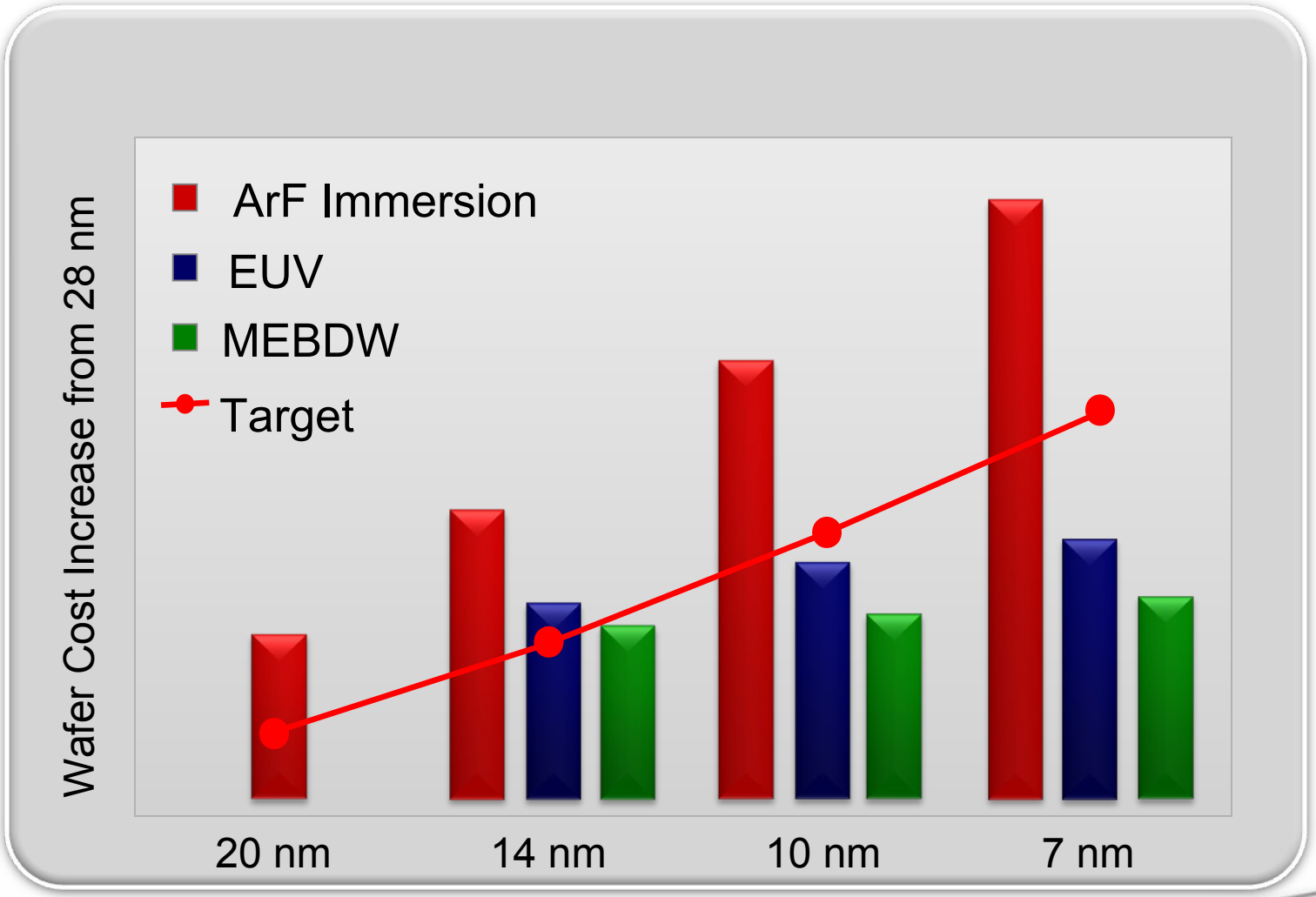


Restricted rules and extended DFM for variability reduction

Why EUVL for 14 nm and Beyond?

TSMC Property

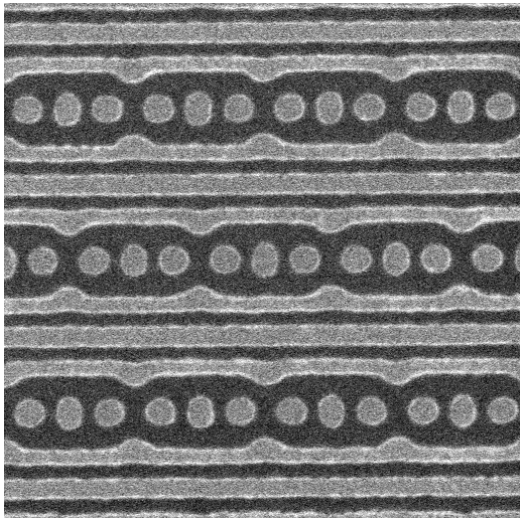
Migration to NGL is necessary to sustain Moore's law economically



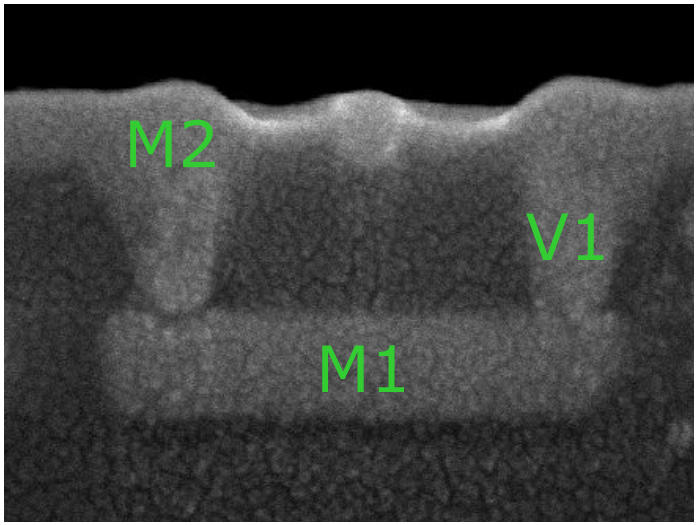
Progress in EUVL Development at TSMC

- Carried out EUV exposure on Alpha Demo Tool at IMEC and ASML Veldhoven with further processing in Taiwan
- Installation of NXE3100 EUV scanner is nearly complete
- Resist screening is being carried out at SEMATECH facilities in Albany and Berkeley
- Mask making technology including patterning, inspection, repair, cleaning, and handling is being developed
  - An R&D mask facility has been established for EUV mask making
  - Mask handling and transportation are being studied

20-nm back-end short-loop wafers processed

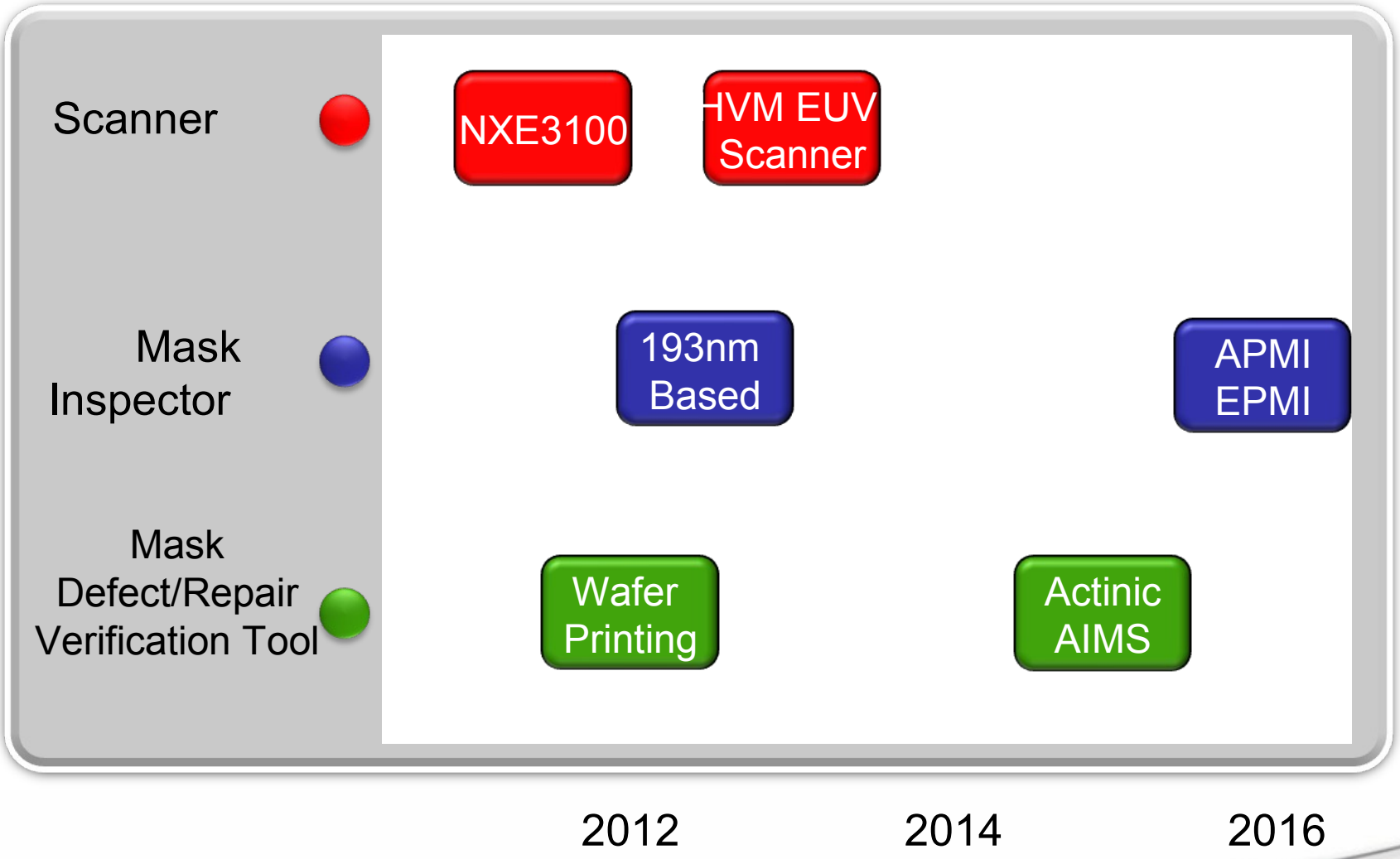


M1 layer patterned by single EUV exposure



Back-end short-loop wafers for WAT

EUVL Infrastructure and Timing



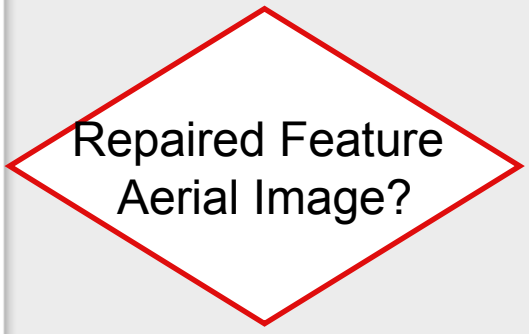
Challenges in Defects Management of EUV Masks

Challenges in Defect Management

Defect Classification

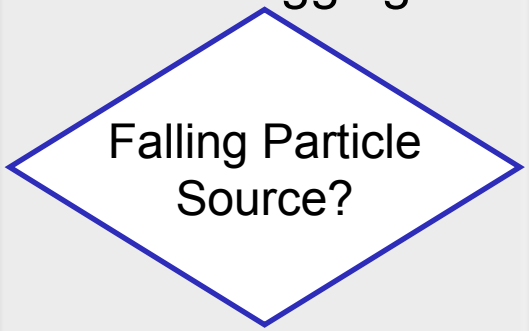
1. Wafer printing
2. Simulated AIMS Images
3. Repair all defects

Repaired Defect Verification



1. Wafer printing
2. Simulated AIMS Images

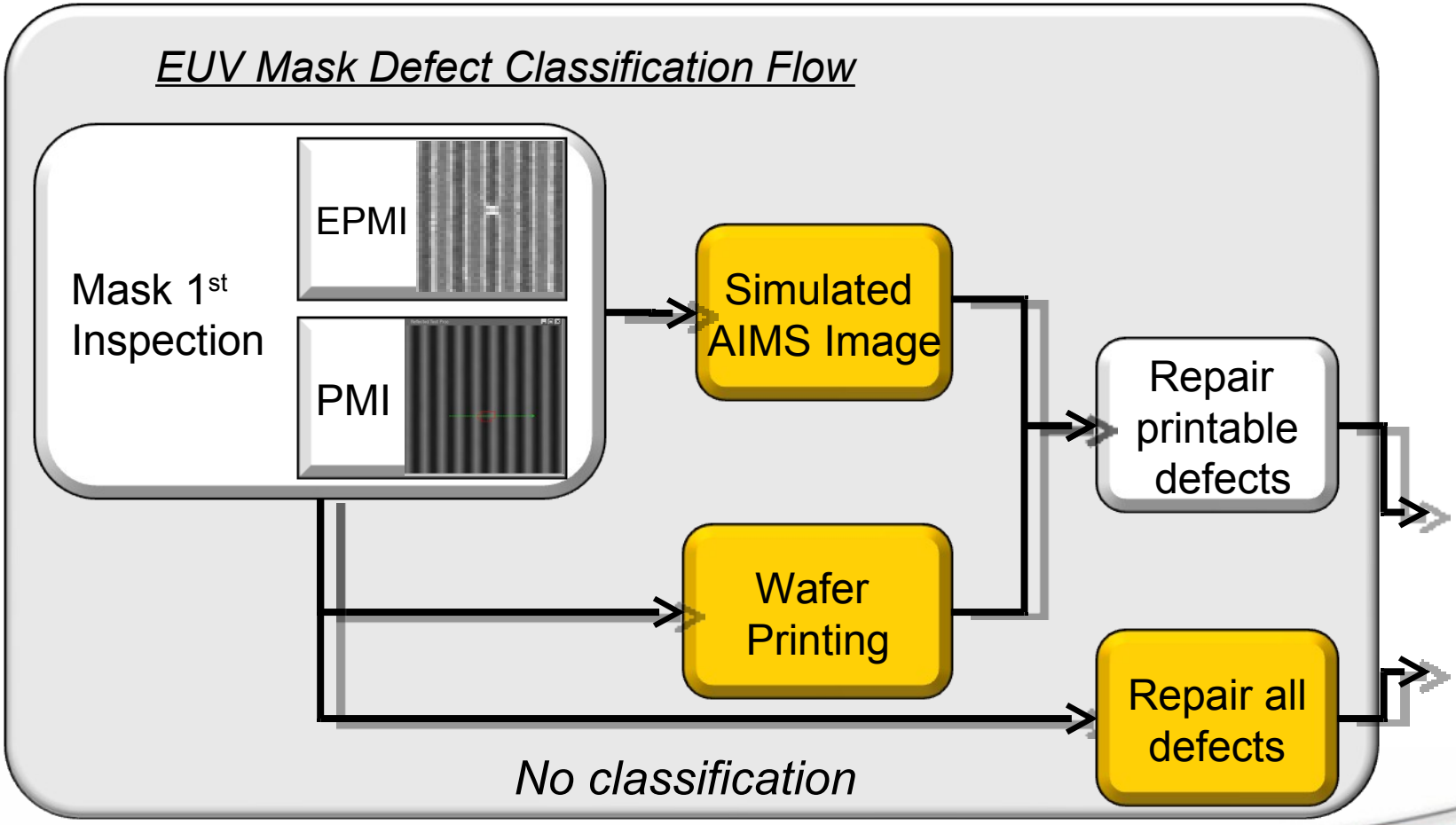
Soft Defect De-Bugging



1. Dual-pod cleanliness inspection
2. How to maintain cleanliness w/o pellicles?

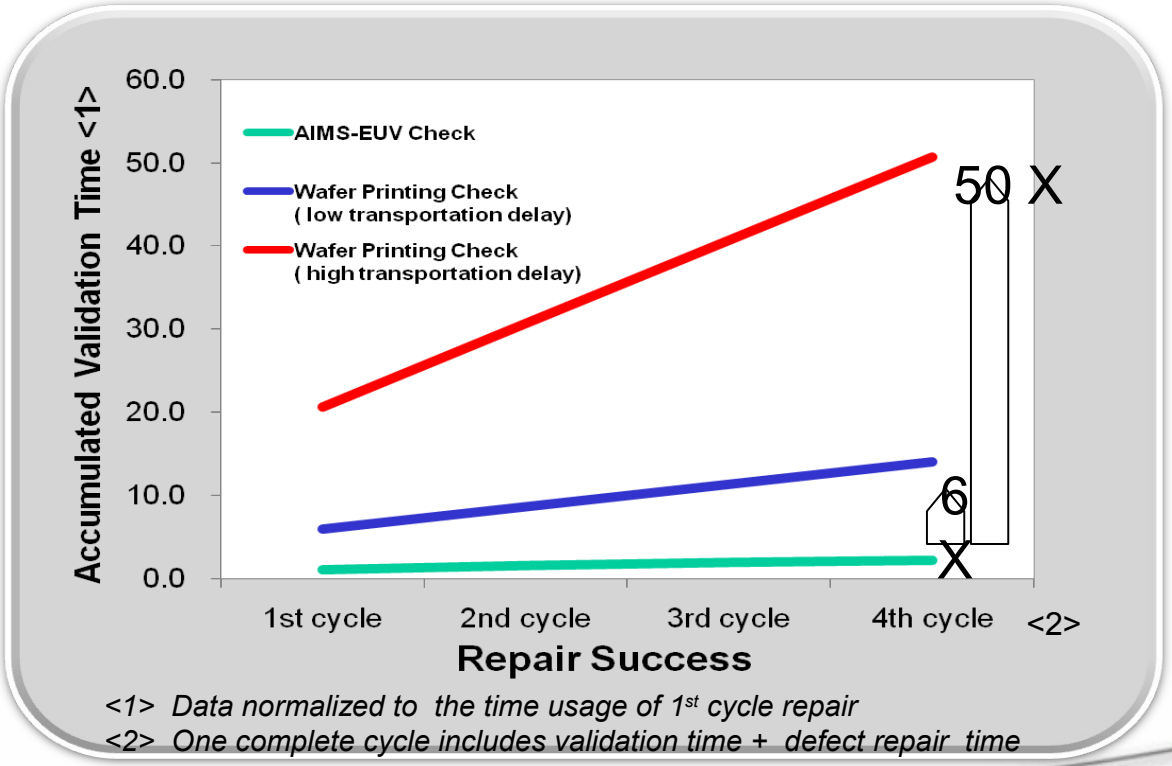
Mask Defect Classification Challenge

Before actinic AIMS becomes available, only wafer printing can perform defect classification after 1st inspection



Repaired Defect Verification Challenge

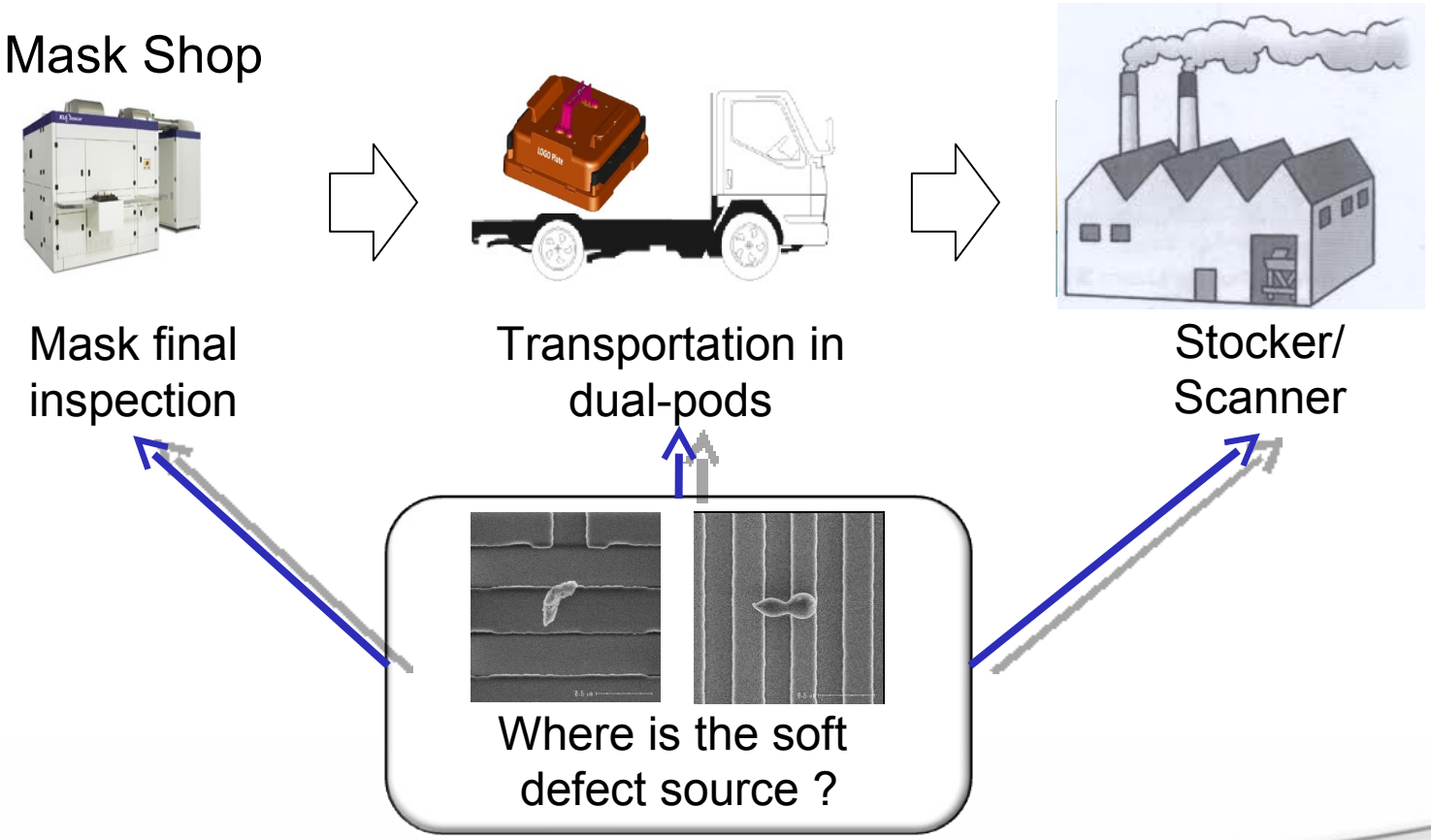
Wafer printing will consume 6X~50X the time required by AIMS-EUV



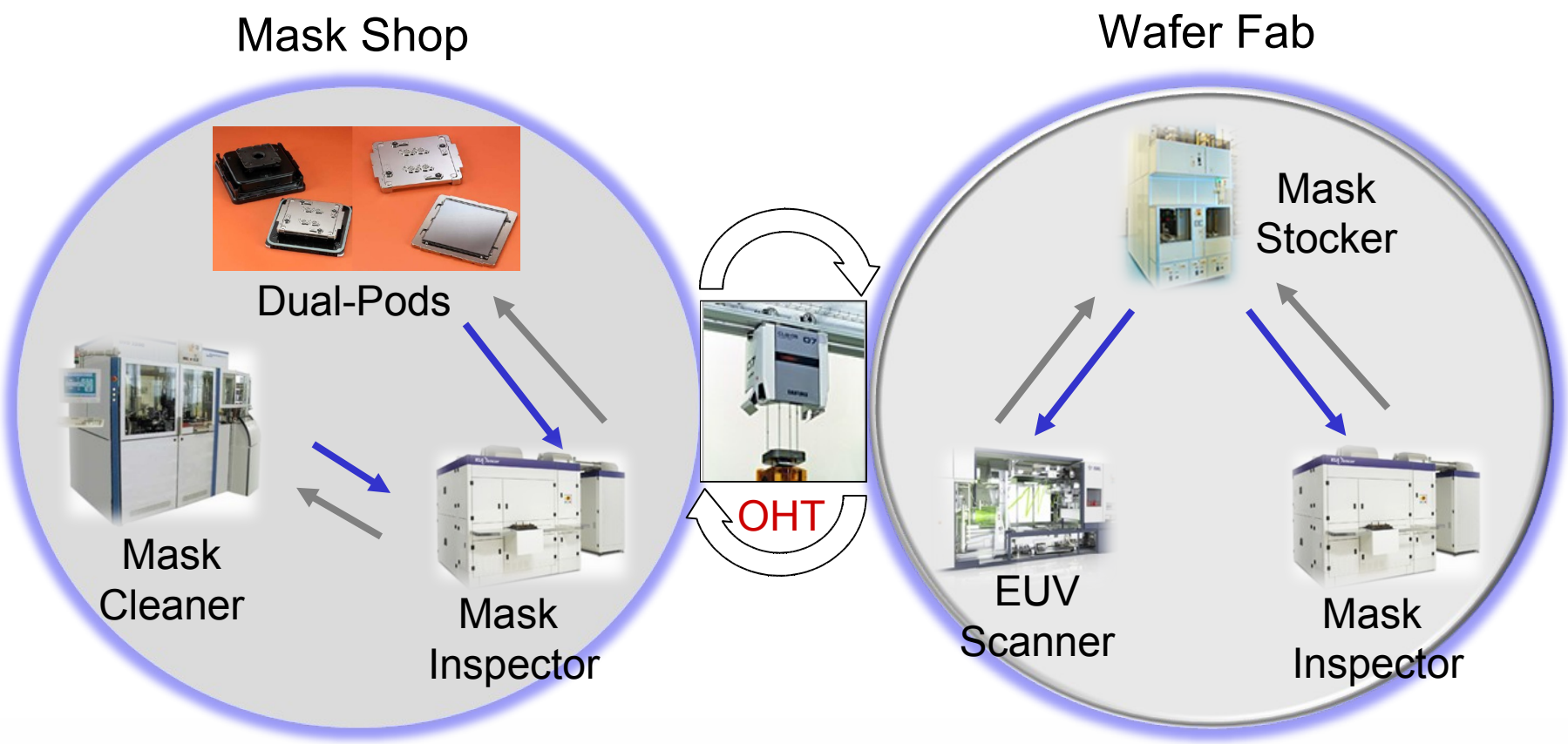
<1> Data normalized to the time usage of 1st cycle repair
<2> One complete cycle includes validation time + defect repair time

Soft Defect De-Bugging Challenge

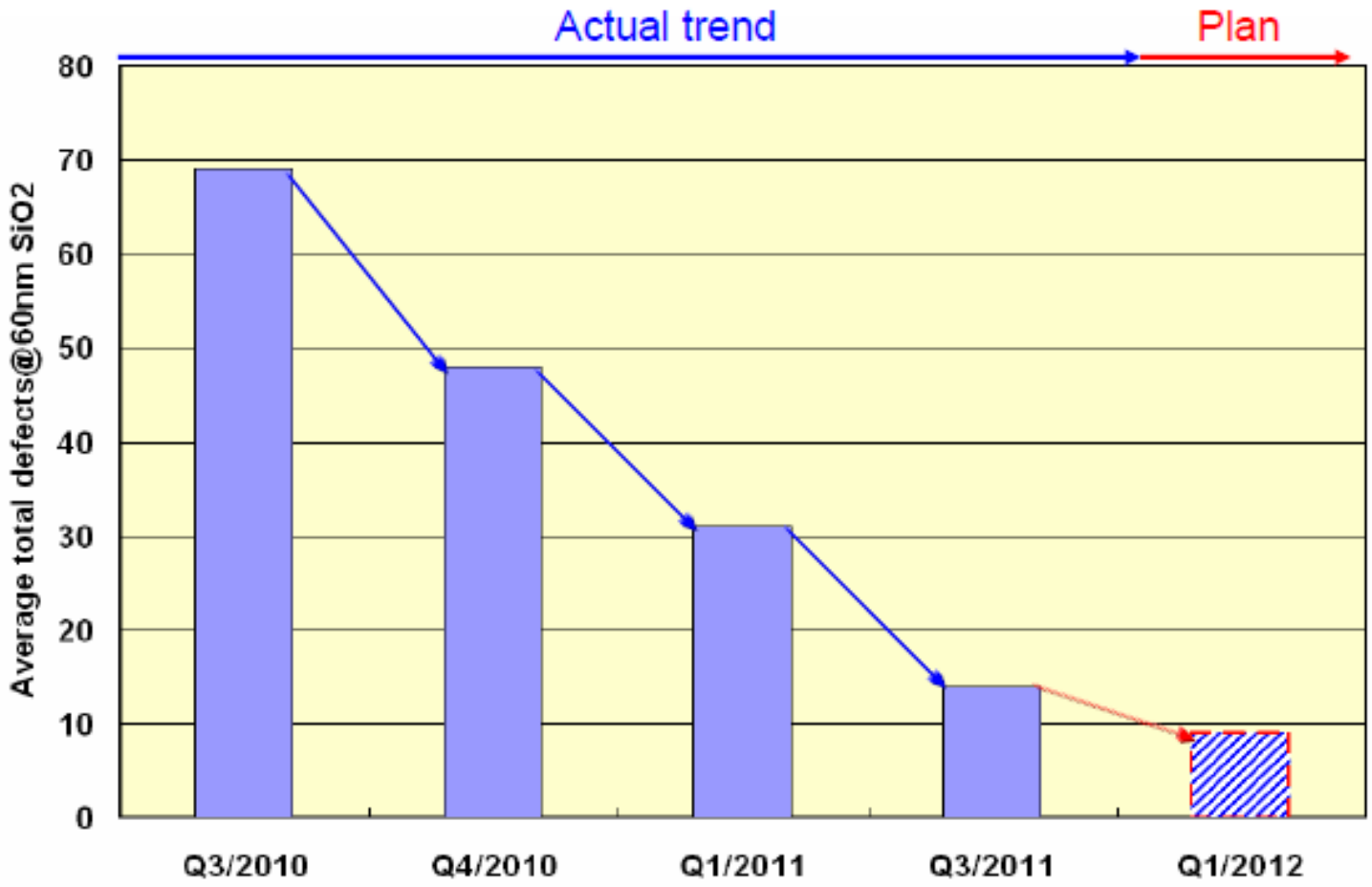
Identifying defect source from completed masks to the scanner is a big challenge once repeating defects are found on wafer



Mask Handling between Mask Shop and Wafer Fab



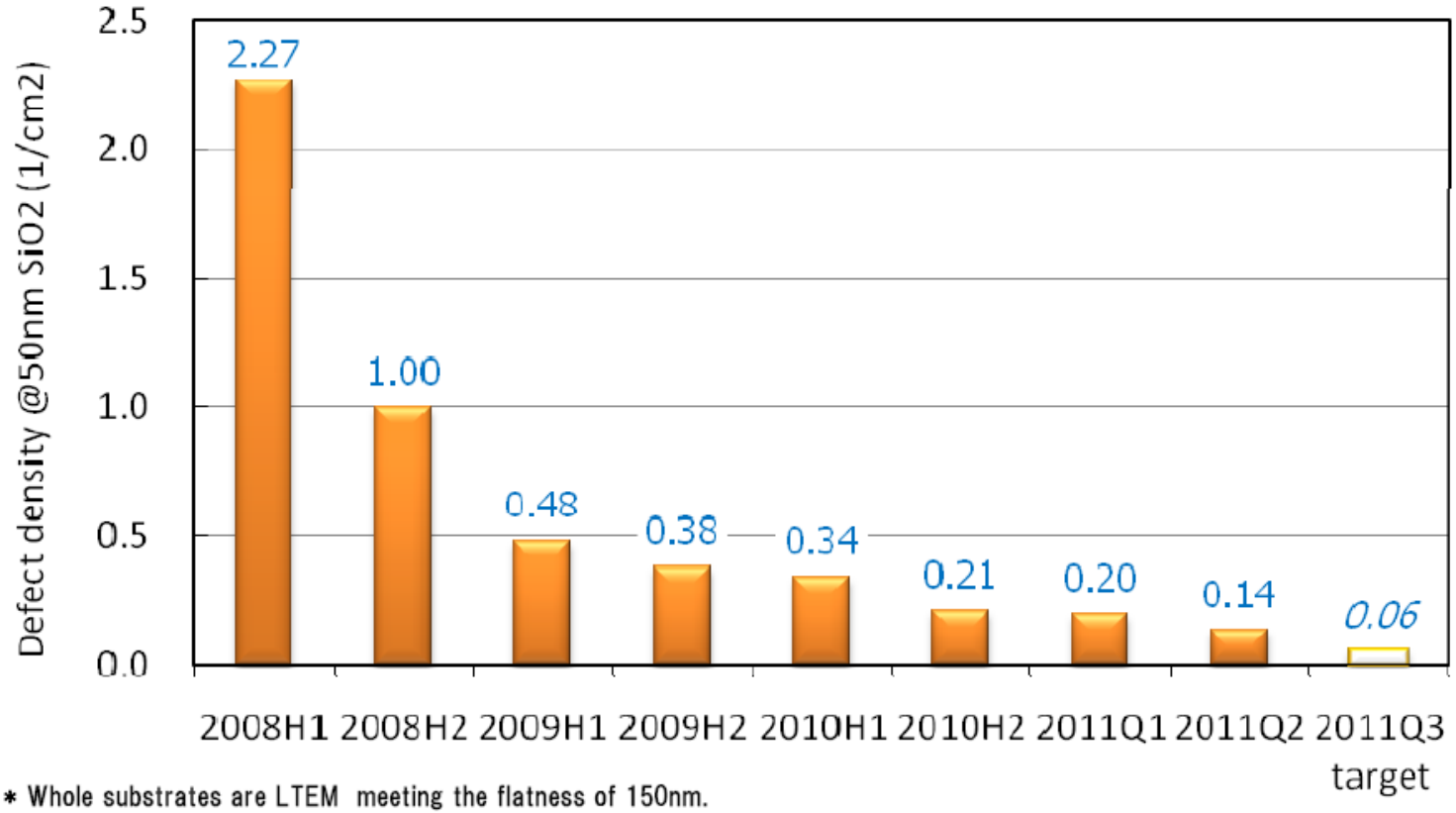
Ru-ML blank defect reduction trend and plan



Courtesy of Hoya

ML blank defect reduction

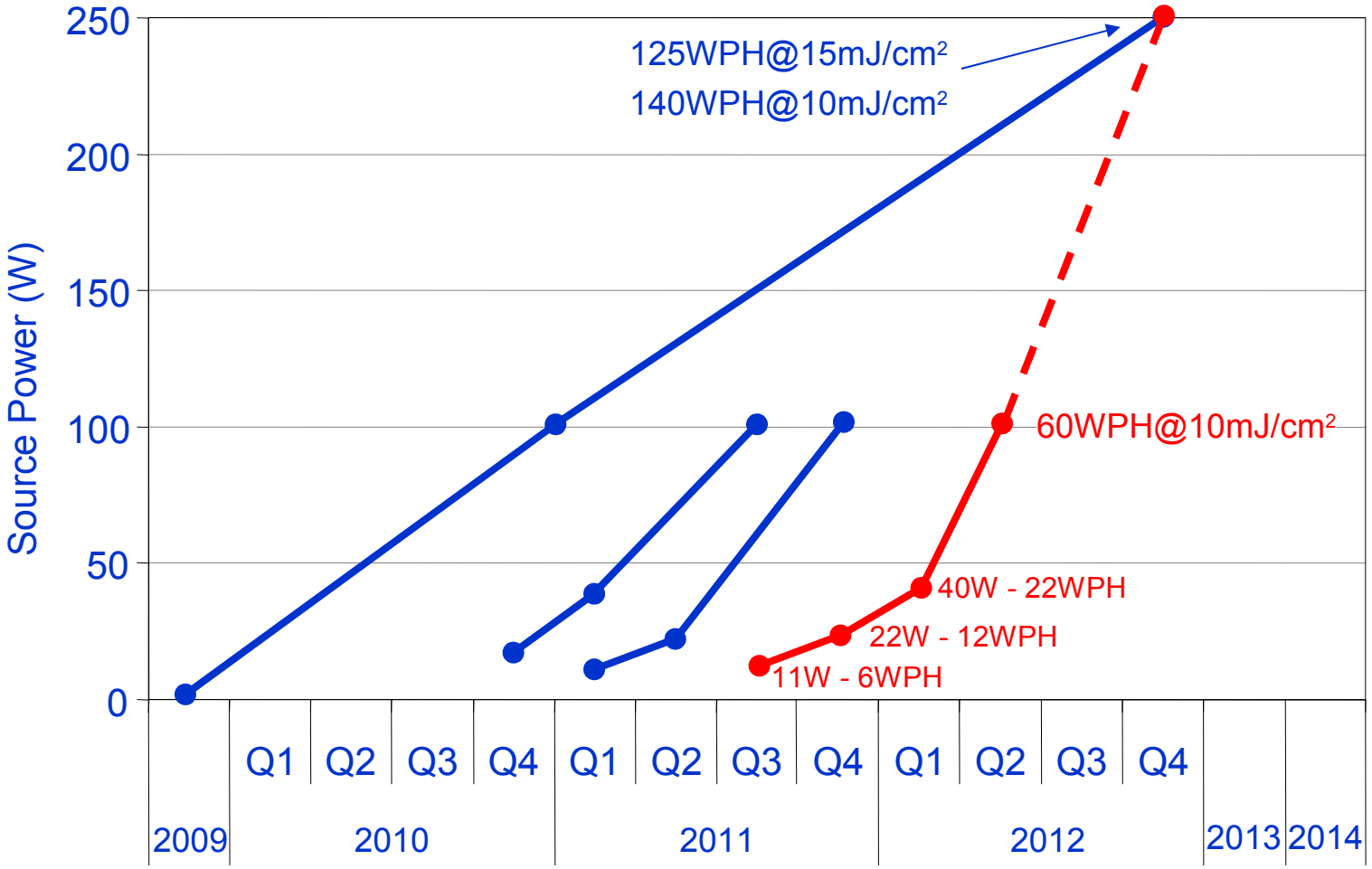
- AGC achieved 0.14/cm2 (24/plate) in 11/Q2, which is 30% less than the last best performance of 0.20/cm2 (34/plate). AGC keeps mitigating the ML
- AGC continuously works out the improvements of Material, Polishing, Cleaning and Coating processes to achieve 11/Q3 target of defect.



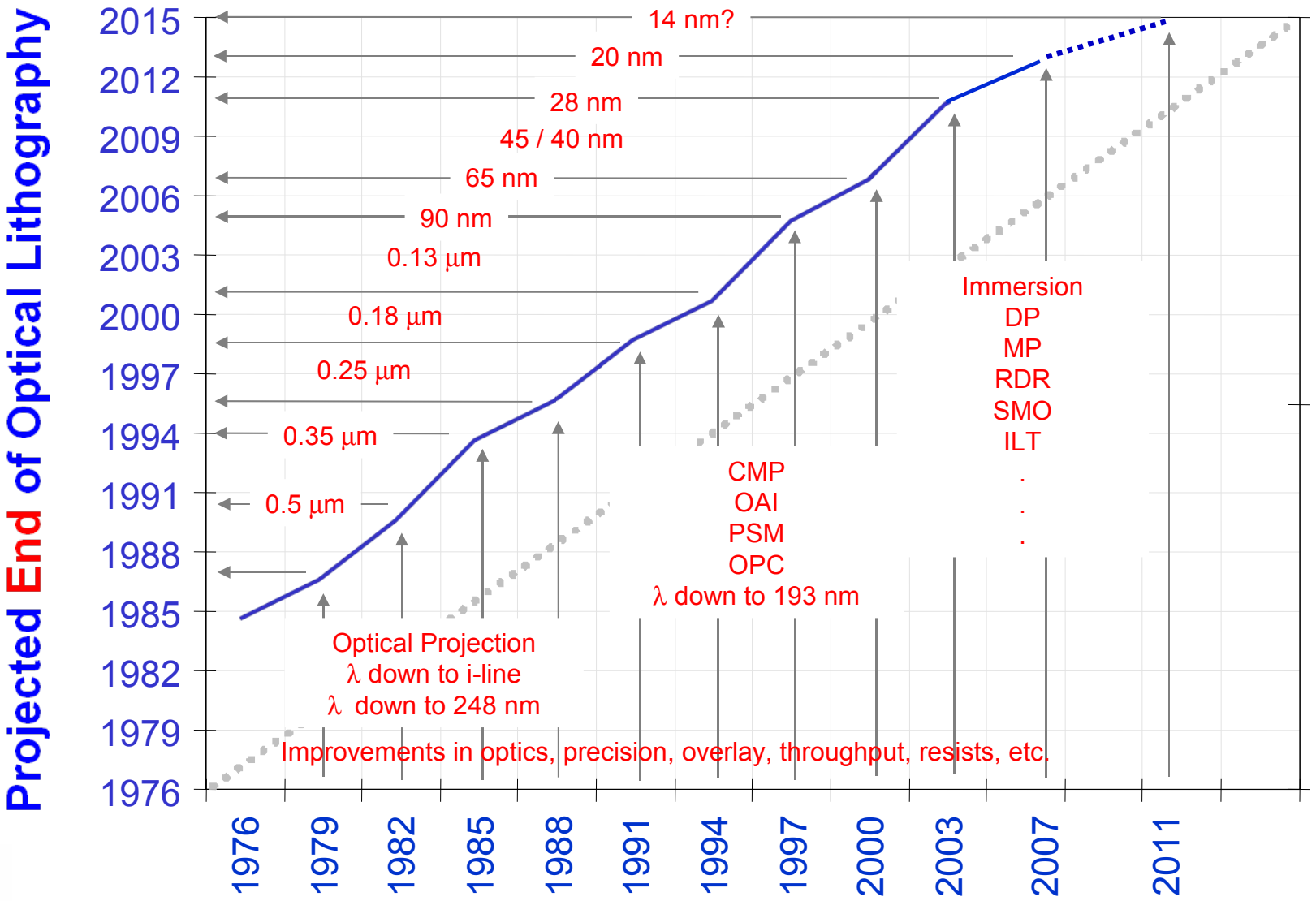
* Whole substrates are LTEM meeting the flatness of 150nm.
* This data was obtained under combined effort with INTEL.cop(USA). The data was disclosed with INTEL's consent.

Courtesy of AGC

Challenges in Delivering Source Power



Can Optical Lithography Be Extended to 14 nm?



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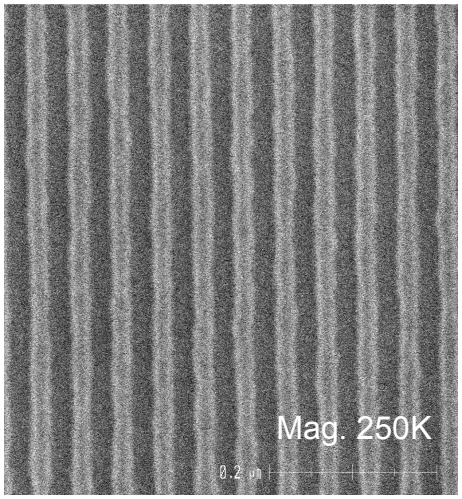
What should this community immediately address

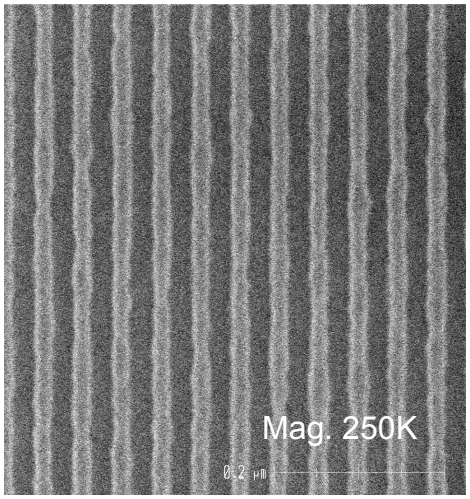
- On-time delivery of HVM scanners w/ good throughput
  - Roadmap slip for EUV sources must stop
- On-time delivery of defect-free EUV mask blanks
  - May have to allow repair to achieve defect-free blanks
  - Blank inspector must be able to provide defect coordinates down to nm accuracy
- New resists having better resolution and sensitivity
  - Need 22-nm half-pitch resolution with < 10 mJ/cm^2 sensitivity
  - New resist platforms for application below 14-nm node

Very Preliminary Results from TSMC's NXE3100

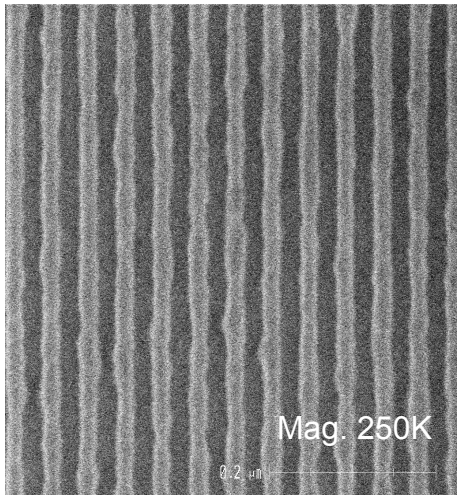
24-nm HP



23-nm HP



22-nm HP



21-nm HP